VOLTAGE MODE OTRA MOS-C SINGLE INPUT MULTI OUTPUT Biquadratic Universal Filter

Rajeshwari PANDEY1, Neeta PANDEY1, Sajal Kumar PAUL2, Ajay SINGH1, Balamurali SRIRAM1, Kaushlendra TRIVEDI1

1Department of Electronics and Communication Engineering, Delhi Technological University, Main Bawana Road 42, Delhi, 110 042, India
2Department of Electronics Engineering, Indian School of Mines, Dhanbad, 826 004, Jharkhand, India

Abstract. In this paper, an Operational transresistance amplifier (OTRA) based MOS-C voltage mode single input multi output (SIMO) biquadratic universal filter configuration is proposed. The configuration is made fully integrated by implementing the resistors using matched transistors operating in the linear region. It exhibits the feature of orthogonal controllability of angular frequency and quality factor through gate bias voltage. The non-ideal analysis of the circuit is also given. Workability of the universal filter is demonstrated through PSPICE simulations using 0.5 μm CMOS process parameters provided by MOSIS (AGILENT).

Keywords
Analog signal processing, OTRA, SIMO, universal filter.

1. Introduction

Recently the OTRA has emerged as an alternate analog building block since it inherits all the advantages offered by current mode techniques. The OTRA is a high gain current input voltage output device. The input terminals of OTRA are internally grounded, thereby eliminating response limitations due to parasitic capacitances and resistances at the input. Several high performance CMOS OTRA topologies have been proposed in literature [1], [2], [3], [4], [5] leading to growing interest in OTRA based analog signal processing circuits. In the recent past, OTRA has been extensively used as an analog building block for realizing a number of analog signal processing and generation circuits such as immittance simulators [6], [7], [8], [9], oscillators [10], [11] multivibrators [12], [13] and filters [1], [14], [15], [16], [17], [18], [19], [20], [21], [22]. Many voltage-mode biquadratic filters using OTRA were proposed in the literature that can be classified as single input and single output (SISO) [1], [13], [14], [15], [16] multi-input single output (MISO) [17], [18], [19], and single input multi output (SIMO) [1], [20]. However, only one standard filter function can be obtained at a time in each filter realization of SISO and MISO category. In SIMO configuration with only one input, multiple filter functions may be obtained simultaneously. A detailed comparison of these structures is given in Tab. 1 which reveals that no OTRA based SIMO structure is available in the literature that provides all five standard responses simultaneously. In this paper, a voltage-mode OTRA MOS-C universal biquadratic SIMO filter based on ref. [1] is presented which realizes all the standard filter functions; namely lowpass, highpass, bandpass, notch and allpass, simultaneously. The proposed structure puts no restriction on the input signal in contrast to the structures reported in [18], [19], [20]. Additionally the earlier reported structures require either change of component type [14], [17] or removal of components [1], [22] for realizing various filter responses. However, the proposed circuit does not require a change in component type/ removal of components. It simply poses matching condition on component values for notch and all pass responses. The proposed OTRA MOS-C universal biquadratic SIMO filter employs five OTRAs, twelve resistors and two capacitors. It also enjoys the feature of orthogonal controllability of angular frequency, quality factor and filter gain. All resistors are implemented using MOS transistors operating in the linear region. This not only makes filter electronically tunable but also consumes less chip area. The function of proposed filter has been confirmed by SPICE simulations.

2. Circuit Description

OTRA is a three terminal device, shown symbolically in Fig. 1. Its port relations are characterized by the
Tab.1: Comparison of the proposed work with the previously reported work.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>No. of inputs</th>
<th>Simultaneous Outputs</th>
<th>Standard filter functions available</th>
<th>Condition</th>
<th>No. of OTRA</th>
<th>No. of passive components (C/R)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[11]</td>
<td>One</td>
<td>Two/Three</td>
<td>LP,BP</td>
<td>No/No</td>
<td>Two</td>
<td>Two/Four</td>
</tr>
<tr>
<td></td>
<td></td>
<td>One</td>
<td>LP,BP</td>
<td>No/Yes</td>
<td>One</td>
<td>LP: Two/Three HP: Three/Two BP: Two/Two NF: AP: Three/Three</td>
</tr>
<tr>
<td>[14]</td>
<td>One</td>
<td>One</td>
<td>LHP,BP,NF,AP</td>
<td>No/No</td>
<td>Two</td>
<td>Two/Four</td>
</tr>
<tr>
<td>[15]</td>
<td>One</td>
<td>One</td>
<td>LHB, BP</td>
<td>No/No</td>
<td>Two</td>
<td>Two/Four</td>
</tr>
<tr>
<td>[16]</td>
<td>One</td>
<td>One</td>
<td>AP</td>
<td>No/No</td>
<td>One</td>
<td>First order AP: One/Three Second order AP: Two/Four</td>
</tr>
<tr>
<td>[17]</td>
<td>One</td>
<td>One</td>
<td>AP,BR</td>
<td>No/Yes</td>
<td>One</td>
<td>1st order AP: One/three or Two/Two 2nd order AP: NF: Three/Three</td>
</tr>
<tr>
<td>[18]</td>
<td>Four</td>
<td>One</td>
<td>LHP,BP,NF,AP</td>
<td>Yes/Yes</td>
<td>Two</td>
<td>Topology 1: Five/Four Topology 2: Six/Four</td>
</tr>
<tr>
<td>[19]</td>
<td>Three</td>
<td>One</td>
<td>LHP,BP,NF,AP</td>
<td>Yes/Yes</td>
<td>One</td>
<td>Four/Four</td>
</tr>
<tr>
<td>[20]</td>
<td>Two</td>
<td>One</td>
<td>LHP,BP,NF</td>
<td>Yes/No</td>
<td>Two</td>
<td>Three/Four</td>
</tr>
<tr>
<td>[21]</td>
<td>One</td>
<td>Three</td>
<td>LHP,BP</td>
<td>No/No</td>
<td>Three</td>
<td>Two/Six</td>
</tr>
<tr>
<td>[22]</td>
<td>One</td>
<td>One</td>
<td>LHP,BP,NF,AP</td>
<td>No/Yes</td>
<td>Three</td>
<td>Two/Eight</td>
</tr>
<tr>
<td>Proposed work</td>
<td>One</td>
<td>Five</td>
<td>LHP,BP,NF,AP</td>
<td>No/Yes</td>
<td>Five</td>
<td>Two/Twelve</td>
</tr>
</tbody>
</table>

following matrix.

\[
\begin{bmatrix}
V_p \\
V_n \\
V_o \\
I_p \\
I_n \\
I_O
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 0 \\
0 & 0 & 0 \\
R_m - R_m & 0 & 0
\end{bmatrix} \begin{bmatrix}
I_p \\
I_n \\
I_O
\end{bmatrix}.
\]  

(1)

Fig. 1: OTRA circuit symbol.

For ideal operations, the transresistance gain \( R_m \) of OTRA approaches infinity and forces the input currents to be equal. Thus, OTRA must be used in a negative feedback configuration. The proposed filter is shown in Fig. 2. Routine analysis of the circuit of Fig. 2 results in the following transfer functions:

\[
V_{01} = \frac{s^2 G_1 C_1 C_2}{D(s)}, \quad (2)
\]

\[
V_{02} = \frac{s G_2 G_4 C_2}{D(s)}, \quad (3)
\]

\[
V_{03} = \frac{G_5 G_6 G_6}{D(s)}, \quad (4)
\]

\[
V_{04} = \frac{G_1}{G_9} \frac{s^2 G_1 C_1 C_2 + \frac{G_5}{G_9} G_5 G_6 G_6}{D(s)}, \quad (5)
\]

\[
V_{05} = \frac{G_1}{G_9} \frac{G_11 + \frac{G_5}{G_9} G_5 G_6 G_6}{G_12}, \quad (6)
\]

where \( D(s) = s^2 G_1 C_1 C_2 + s G_2 G_4 C_2 + G_5 G_6 G_6 \).

Equations (2)–(4) clearly indicate that high pass, band pass, low pass responses are available at \( V_{01} \), \( V_{02} \), and \( V_{03} \) respectively. Band reject response is available at \( V_{04} \) as given in (5), with BR gain \( G_{BR} = G_1 / G_5 \), if

\[
G_7 = G_9, \quad G_1 G_6 = G_2 G_9.
\]  

(7)

An allpass response is available at \( V_{05} \), as expressed in (6) with allpass gain \( G_{AP} = G_1 / G_3 \), if

\[
G_7 G_{10} = G_5 G_{12}, \quad G_7 G_11 = G_6 G_{12}, \quad G_5 G_6 G_{11} = G_2 G_9 G_{12}.
\]  

(8)

The high pass gain \( G_{HP} \), band pass gain \( G_{BP} \) and the low pass gain \( G_{LP} \) are respectively given by

\[
G_{HP} = G_1 / G_3, \quad G_{BP} = G_1 / G_5, \quad G_{LP} = G_1 / G_2.
\]  

(9)

The resonant angular frequency \( \omega_0 \) and the quality factor \( Q_0 \) are given by:

\[
\omega_0 = \frac{G_2 G_5 G_6}{\sqrt{C_1 C_2 C_3}}, \quad (10)
\]

\[
Q_0 = \frac{G_2 G_5 G_6}{\sqrt{C_1 C_2 C_3}}.
\]
This suggests that the \( Q_0 \) can be independently controlled by varying \( R_2 \) without affecting the \( \omega_0 \). It can be noted from (10) that simultaneous adjustment of \( R_2 \) and \( R_1 \) results in orthogonal tuning of \( \omega_0 \). Also, the filter gain can be controlled through \( R_1 \) without affecting \( \omega_0 \) and \( Q_0 \).

The sensitivities of \( \omega_0 \) and \( Q_0 \) with respect to each passive component are low and obtained as

\[
S_{R_2}^{\omega_0} = S_{R_4}^{\omega_0} = S_{R_6}^{\omega_0} = \frac{1}{2}, \quad S_{R_3}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2}. \tag{12}
\]

\[
S_{R_2}^{Q_0} = -1, \quad S_{R_4}^{Q_0} = S_{R_6}^{Q_0} = S_{R_3}^{Q_0} = S_{C_1}^{Q_0} = S_{C_2}^{Q_0} = -\frac{1}{2}. \tag{13}
\]

It is well known that the linear passive resistor consumes a large chip area as compared to the linear resistor implementation using transistors operating in the linear region. The differential input of OTRA allows the resistors connected to the input terminals of OTRA to be implemented using MOS transistors with complete non-linearity cancellation [1]. Figure 3 shows a typical MOS implementation of resistance connected between negative input and output terminals of OTRA. The resistance value may be adjusted by appropriate choice of gate voltages thereby making filter parameters electronically tunable. The value of resistance so obtained is expressed as

\[
R = \frac{1}{\mu_n C_{ox}(W / L)(V_u - V_b)}.
\tag{14}
\]

where \( \mu_n \), \( C_{ox} \), \( W \) and \( L \) are electron mobility, oxide capacitance per unit gate area, effective channel width, and effective channel length of MOS respectively which may be expressed as

\[
\mu_n = \frac{\mu_0}{1 + \theta(V_{GS} - V_T)}.
\tag{15}
\]

V\(_g\) and V\(_b\) are the gate voltages and other symbols have their usual meaning. Figure 4 shows the MOS-C implementation of the circuit of Fig. 2.

3. Non-Ideality Analysis

The response of the filter may deviate due to non-ideality of OTRA in practice. Ideally the trans-resistance gain \( R_m \) is assumed to approach infinity. However, practically \( R_m \) is a frequency dependent finite value. Considering a single pole model for the trans-resistance gain, \( R_m \) can be expressed as

\[
R_m(s) = \left( \frac{R_0}{1 + s / \omega_0} \right), \tag{19}
\]

where \( R_0 \) is low frequency transresistance gain. For high frequency applications, the transresistance gain, \( R_m(s) \) reduces to

\[
R_m(s) \approx \frac{1}{sC_p} \text{ where } \quad C_p = \frac{1}{R_0 \omega_0}. \tag{20}
\]

Taking this effect into account the transfer functions of the circuit of Fig. 3 modify to
Fig. 4: OTRA MOS-C universal filter.

\[
\frac{V_{01}}{V_{in}} = \frac{s^2G_1(C_1 + C_p)(C_2 + C_p)}{D_n(s)},
\]

(21)

\[
\frac{V_{02}}{V_{in}} = \frac{sG_1G_4(C_2 + C_p)}{D_n(s)},
\]

(22)

\[
\frac{V_{03}}{V_{in}} = \frac{G_4G_5G_6}{D_n(s)},
\]

(23)

\[
\frac{V_{04}}{V_{in}} = \frac{G_1}{D_n(s)(G_9 + sC_p)},
\]

(24)

\[
(V_2 + C_p)(A s^2(C_1 + C_p) - G_4G_1) + \frac{G_4G_5G_6G_1}{(G_9 + sC_p)}
\]

(25)

where \( A = \frac{G_2G_1}{G_3G_1} \) and \( D_n(s) = s^2(G_3 + sC_p)(C_1 + C_p)(C_2 + C_p) + sG_4G_5(C_2 + C_p) + G_4G_5G_6 \)

(26)

4. Simulation Results

The proposed SIMO biquadratic universal filter is verified through simulations using the CMOS implementation of the OTRA [3] as given in Fig. 5. The SPICE simulation was performed using 0.5 µm CMOS process parameters provided by MOSIS (AGILENT). Supply voltages taken are ±1.5 V. Aspect ratios for different transistors used in OTRA are given in Tab. 2. For simulations \( L_{drawn} \) and \( W_{drawn} \) are taken as 5 µm for all transistors used for resistance realization.

Fig. 5: CMOS implementation of OTRA [3].

Tab.2: Aspect ratio of transistors used in OTRA.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W(µm)/L(µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M3</td>
<td>100/2.5</td>
</tr>
<tr>
<td>M4</td>
<td>10/2.5</td>
</tr>
<tr>
<td>M5,M6</td>
<td>30/2.5</td>
</tr>
<tr>
<td>M7</td>
<td>10/2.5</td>
</tr>
<tr>
<td>M8-M11</td>
<td>50/2.5</td>
</tr>
<tr>
<td>M12,M13</td>
<td>100/2.5</td>
</tr>
<tr>
<td>M14</td>
<td>50/0.5</td>
</tr>
</tbody>
</table>

The proposed SIMO biquadratic universal filter as given in Fig. 4 is designed for the resonant frequency \( f_0 \) of 120 kHz and \( Q_0=1 \) with component values \( C_1=C_2=100 \) pF and \( R_i \approx 10.5 \) kΩ for \( i = 1, 2, \ldots, 12. \)
The value of $R_i$ was set by taking the gate voltages as $V_{ai} = 1.4$ V and $V_{bi} = 0.75$ V for all $i = 1, 2, \ldots, 12$. Figure 6 shows the simultaneously available frequency responses for low-pass, high-pass, band-pass, notch and all-pass. The simulated resonant frequency is found to be in close agreement to the theoretical value. The orthogonal tunability of $Q_0$ with $R_5$ at $f_0 = 11.5$ kHz is shown in Fig. 7. This is obtained by selecting $C_1 = C_2 = 50$ pF and $R_5 = 272$ kΩ for $i = 1, \ldots, 3, 5, \ldots, 12$, along with different gate voltages chosen for varying $R_4$ are listed in Tab. 4.

The $f_0$ is electronically tunable by varying the gate voltage and is verified through simulations as depicted in Fig. 8. Values of $f_0$ for $C_1 = C_2 = 50$ pF and $R_5 = 23$ kΩ for $i = 1, \ldots, 3, 5, \ldots, 12$, along with different gate voltages chosen for varying $R_4$ are listed in Tab. 4.

To study the time domain behavior of the BP filter three sinusoidal frequency components, a low frequency signal of 1 kHz, a high frequency component of 100 kHz and the third component is 11.5 kHz which is $f_0$ of the BP filter, are applied. The transient response of the filter circuit is shown in Fig. 9. It may be noted that the

![Fig. 6: Simulated frequency responses of the proposed circuit (a) low-pass and high-pass, (b) band-pass and notch, (c) all pass.](image1)

![Fig. 7: Band-pass response for different $Q_0$ values.](image2)

![Fig. 8: Notch response for different $\omega_0$ values.](image3)

![Fig. 9: Transient response of the filter circuit.](image4)
frequency components other than $f_0$ are significantly attenuated.

Fig. 9: Simulated transient response of BP filter. (a) Input signal and its frequency response (b) Output transient response and frequency spectrum.

To check the quality of the output of BP filter, the percentage total harmonic distortion (%THD) with the sinusoidal input signal is obtained as shown in Fig. 10. It is observed that the %THD remains considerably low [23] for input signal values till 70 mV. Simulated power consumption for the proposed universal filter is 4.04 mW.

Fig. 10: THD variation with the input signal amplitude.

5. Conclusion

A new voltage-mode OTRA MOS-C universal biquadratic filter is presented which realizes all the standard filter functions simultaneously. The proposed circuit employs five OTRAs, two capacitors and twelve resistors. The filter possesses orthogonal and electronic tunability of filter parameters through MOS implemented resistors. The theoretical proposition is verified using PSPICE simulations.

References


About Authors

Rajeshwari PANDEY did B.Tech. (Electronics and Telecommunication) from University of Allahabad in 1988 and received her M.E (Electronics and Control) from BITS, Pilani, Rajasthan, India in 1992. Currently, she is Associate Professor in Department of Electronics and Communication Engineering, Delhi Technological University, Delhi. Her research interests include Analog Integrated Circuits, and Microelectronics.

Neeta PANDEY did M. E. in Microelectronics from Birla Institute of Technology and Sciences, Pilani, Rajasthan, India and Ph.D. from Guru Gobind Singh Indraprastha University Delhi, India. At present she is Associate Professor in Department of Electronics and Communication Engineering, Delhi Technological University, Delhi. A life member of ISTE, and member of IEEE, USA, she has published papers in International, National Journals of repute and conferences. Her research interests are in Analog and Digital VLSI Design.

Sajal Kumar PAUL did B.Tech., M.Tech., and Ph.D. in Radio Physics and Electronics from the Institute of Radio Physics and Electronics, University of Calcutta. He has served Webel Telecommunication Industries, Kolkata; Indira Gandhi National Open University (IGNOU), Kolkata; Advanced Training Institute for Electronics &Process Instrumentation (ATI-EPI), Hyderabad; North Eastern Regional Institute of Science & Technology (NERIST), Nirjuli and Delhi College of Engineering (DCE), Delhi in various capacities. He has served the Department of Electronics Engineering, Indian School of Mines, Dhanbad as Head of the Department and at present professor of the same department. His research interest includes Microelectronic Devices, Electronic Properties of Semiconductor and Bipolar and MOS Analog Integrated Circuits. He has more than 60 research publications in International and National journals of repute and conferences.

Ajay SINGH completed B. E. degree in June 2012 from Delhi Technological University, Delhi, India. His main research Interests include the field of analog circuit design and Signal processing. He has published few papers in National and International conferences/
journals.

Balamurali SRIRAM completed B. E. degree in June 2012, from Delhi Technological University, Delhi, India. His research interests include mixed signal circuit design and analog signal processing. Has also co-authored a journal and conference papers.

Kaushalendra TRIVEDI completed B. E. degree in June 2012 from Delhi Technological University, Delhi, India. His research interests include mixed signal circuit design and signal processing. Has also co-authored a journal and conference papers in current mode circuits.